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## APPLICANTS

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## \*\* CONTINUING DATA \*\*\*\*\*

This application is a DIV of 09/970,758 10/04/2001 PAT 6,649,477

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## \*\* FOREIGN APPLICATIONS \*\*\*\*\*

## IF REQUIRED, FOREIGN FILING LICENSE GRANTED

\*\* 02/10/2004

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	STATE OR	SHEETS	TOTAL	INDEPENDENT
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance	COUNTRY	DRAWING	CLAIMS	CLAIMS
Verified and Acknowledged Examiner's Signature <u>TL</u> Initials	CA	8	18	4

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## TITLE

Method for fabricating a power semiconductor device having a voltage sustaining layer with a terraced trench facilitating formation of floating islands

FILING FEE

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 856

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